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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,522	07/08/2003	Jeremy A. Theil	MICR-153US	9342

68551 7590 01/28/2008

RatnerPrestia
P.O. BOX 980
VALLEY FORGE, PA 19482

EXAMINER	
SELBY, GEVELL V	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
01/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/615,522	THEIL ET AL.	
	Examiner	Art Unit	
	Gevell Selby	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,18,19* is/are rejected.

7)☒ Claim(s) *17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, and 5-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Wesfield, US 6,856,351.

In regard to claim 1, Wesfield, US 6,856,351, discloses an image sensor, comprising:

multiple pixels (see figure 2: pixel circuit array) each include a respective photodiode region (see figure 2, element 216) (see column 4, lines 20-27);

pixel circuits (see figure 3) each operable to control integration and readout steps for a respective pixel (see column 4, lines 34-45); and

a bias circuit (see figure 3, elements 310, 312, 314) operable to apply voltages across the pixels to induce carrier injection into the photodiode regions to reduce image lag (see column 4, line 42-57: It is inherent that applying the

voltage across the pixel element 316 in the Wesfield reference induces carrier injection into the photodiode region, since the lag is reduced).

In regard to claim 2, Wesfield, US 6,856,351, discloses the image sensor of claim 1, wherein the bias circuit is operable to induce forward bias flow of injected carriers through the pixel photodiode regions (see column 4, lines 52-54).

In regard to claim 5, Wesfield, US 6,856,351, discloses the image sensor of claim 2, wherein pixels are arranged in an array of multiple rows (see column 2, lines 41-51) and the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions of all pixels in a given row of the array (see column 4,lines 52-54: It is inherent the bias circuit of the Wesfield reference is operable to induce the bias in all the pixels of a row, since each diode is switched on under high illumination).

In regard to claim 6, Wesfield, US 6,856,351, discloses the image sensor of claim 5, wherein the bias circuit is operable to simultaneously induce forward bias flow of injected carriers through the photodiode regions one row at a time (see column 4,lines 52-54: It is inherent the bias circuit of the Wesfield reference is operable to induce the bias in one row at a time, since each diode is switched on under high illumination).

In regard to claim 7, Wesfield, US 6,856,351, discloses the image sensor of claim 6. It is inherent the bias circuit of the Wesfield reference is operable to simultaneously induce forward bias flow of injected carriers through photodiode regions of a given row before the pixel circuits in the given row initiate an integration step for the given row,

because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 8, Wesfield, US 6,856,351, discloses the image sensor of claim 5. (see column 4, lines 52-54: It is inherent the bias circuit of the Wesfield reference is operable to simultaneously induce forward bias flow of injected carriers through photodiode regions of all rows in the array, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed, since each diode is switched on under high illumination, such that when all the pixel are under high illumination, all the diodes are switched on).

In regard to claim 9, Wesfield, US 6,856,351, discloses the image sensor of claim 1, wherein it is inherent the Zhao reference discloses that the bias circuit is operable to induce carrier injection between photodiode regions of pixels, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 10, Wesfield, US 6,856,351, discloses the image sensor of claim 1, wherein it is inherent the Zhao reference discloses that the bias circuit is operable to induce carrier injection between photodiode regions of adjacent pixels, because this is an intended use of the bias circuit and the structure of the bias circuit is disclosed.

In regard to claim 11 Wesfield, US 6,856,351, discloses the image sensor of claim 10, wherein the bias circuit is operable to apply different voltages levels to nodes of adjacent pixels (see column 4, lines 46-57).

In regard to claim 12, Wesfield, US 6,856,351, discloses the image sensor of claim 11, wherein the bias circuit is operable to apply different high-to-low voltage ranges across adjacent pixels (see column 4, lines 46-57).

In regard to claim 13, Wesfield, US 6,856,351, discloses the image of sensor of claim 11, wherein pixels are arranged in an array of multiple rows (see column 2, lines 41-51) and the bias circuit is operable to apply different voltage levels to nodes of adjacent pixels in adjacent rows (see column 4, lines 46-57: one row may be switches to forward bias while the adjacent is not).

In regard to claim 14, Wesfield, US 6,856,351, discloses the image sensor of claim 11, wherein pixels are arranged in an array of rows and columns (see column 2, lines 41-51) and the bias circuit is operable to apply different voltage levels to nodes adjacent pixels in adjacent rows and to apply different voltage levels to nodes of adjacent pixels in adjacent columns (see column 4, lines 46-57: one row or column may be switches to forward bias while the adjacent is not).

In regard to claim 15, Wesfield, US 6,856,351, discloses the image sensor of claim 10. It is inherent the pixel circuit of the Wesfield reference periodically switches the different voltage levels applied to nodes of adjacent pixels when switching between switching between image sensing, readout, and resetting, in order to properly operate the image sensor to produce the image signals.

In regard to claim 16, Wesfield, US 6,856,351, discloses the image sensor of claim 10, wherein the bias circuit includes two bias lines for applying different respective voltage levels to the pixels (see figure 3, elements 310 and 314).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wesfield, US 6,856,351, in view of Takada et al. US 2001/0015404.

In regard to claim 3, Wesfield, US 6,856,351, discloses the image sensor of claim 2. The Wesfield reference does not specifically disclose wherein the bias circuit is operable to periodically induce forward bias flow of injected carriers through photodiode regions.

Takada et al. US 2001/0015404, discloses an image sensor that periodically applies a forward bias to the phototransistor Ptr during the reset period (see para 256-258).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Wesfield, US 6,856,351, in view of Takada et al. US 2001/0015, to have the bias circuit operable to periodically induce forward bias flow of injected carriers through photodiode regions, in order to correct variations in outputs of individual pixels thus improving the output reliability.

In regard to claim 4, Wesfield, US 6,856,351, in view of Takada et al. US 2001/0015, discloses the image sensor of claim 3. The Takada reference discloses

wherein the pixel circuits and the bias circuit are cooperatively configured so that forward bias flow of injected carriers occurs during a reset step for each pixel (see para 256-258).

6. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wesfield, US 6,856,35.

In regard to claim 18, Wesfield, US 6,856,351, discloses a method of operating an image sensor comprising multiple pixels each including a respective photodiode region (see figure 3 and see column 2, lines 41-51), the method comprising:

resetting photodiode regions (see column 6, lines 8-13);

integrating charge in photodiode regions (see column 6, lines 8-13);

sampling pixel nodes (see column 5, line 58 to column 6, line 2).

The reference discloses in another embodiment applying voltages across the pixels to induce carrier injection into photodiode regions to reduce image lag (see column 4, line 42-57: It is inherent that applying the voltage across the pixel element 316 in the Wesfield reference induces carrier injection into the photodiode region, since the lag is reduced).

It would have been obvious to one of ordinary skill in the art at the time of invention to have been motivated to modify Wesfield, US 6,856,35, to have applying voltages across the pixels to induce carrier injection into photodiode regions to reduce image lag, in order to recover from any illumination level without significant lag.

In regard to claim 19, Wesfield, US 6,856,351, discloses the method of claim 18, wherein inducing carrier injection comprises inducing forward bias flow of carriers through the pixel photodiode regions (see column 4, lines 52-54).

Allowable Subject Matter

7. Claims 17 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gevell Selby whose telephone number is 571-272-7369. The examiner can normally be reached on 8:00 A.M. - 5:30 PM (every other Friday off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on 571-272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

gvs

LIN YE
SUPERVISORY PATENT EXAMINER